ABSTRACT OF THE DISCLOSURE

There is provided a semiconductor integrated circuit device which has realized high speed operation, high integration density and highly efficient layout of the RAM macro, in which a memory array which is divided into four sections in the X and Y coordinates directions is disposed, a first input circuit for receiving a signal which requires optimization for a signal delay is disposed to the center of such four memory arrays, a second input circuit for receiving a data input and control signals thereof is disposed to the center of Y coordinate corresponding to the extending direction of the word line and a signal line for transferring an input signal from the external circuit of the RAM macro to the first and second input circuits is formed using an upper layer wiring for the wiring to form the memory array.